WHAT IS CLAIMED IS:

1. A memory system comprising:

a primary memory controller;

a memory data bus, having an effective bit-width m, coupled to the primary memory controller; and

at least one memory module coupled to the memory data bus, the memory module having a module data bus with an effective bit-width $N = R \times m$, where R is an integer value greater than one, the memory module comprising an interface circuit coupled between the memory data bus and the module data bus, the interface circuit capable of performing m-bit-wide data transfers on the memory data bus, the interface circuit capable of performing N-bit-wide data transfers on the module data bus.

2. The memory system of claim 1, wherein the memory data bus comprises a point-to-point bus having one data bus segment connecting the primary memory controller and the first of the at least one memory modules, and one additional segment for each additional memory module, the additional segment connecting the additional memory module to the module immediately preceding it.

3. The memory system of claim 2, the memory data bus further comprising a ring data bus segment connecting the last of the memory modules in the memory system back to the primary memory controller.

4. The memory system of claim 1, the memory data bus and the module data bus each having a clock rate, the memory data bus clocking at a rate R times the clock rate of the module data bus.

5. A memory module comprising:

R ranks of memory devices, where *R* is at least two, each rank having an *m*-bit-wide data port;

a module data port capable of exchanging data signaling over a memory data bus having an effective bit-width *m*;

an interface circuit coupled between the module data port and the *R* memory-device-rank data ports, the interface circuit capable of performing *m*-bit-wide data transfers at the module data port, the interface circuit capable of performing $R \times m$ -bit-wide data transfers with the *R* ranks of memory devices; and

a controller capable of synchronizing the operation of the interface circuit and the memory device ranks such that a data transfer comprising *R* serial data transfers on the memory data bus can be completed internal to the memory module with one $R \times m$ -bit-wide data transfer with the memory device ranks.

6. The memory module of claim 5, wherein the interface circuit comprises:

R *m*-bit-wide data registers, each register capable of exchanging point-to-point data signaling with a corresponding rank of memory devices through the data port of that rank; and

a multiplexer, having a multiplexing ratio *R*, coupled between the *R* data registers and the external data port.

7. The memory module of claim 6, wherein the controller supplies rank selection signals to the multiplexer and register latching signals to each of the data registers.

8. The memory module of claim 6, wherein data signaling between a data register and its rank of memory devices further comprises a bit mask received from the memory data bus along with a corresponding *m* bits, the multiplexer transferring the bit mask to the data register along with the corresponding *m* bits.

9. The memory module of claim 6, the controller capable of synchronizing the operation of the data registers, the module data port, and the multiplexer/demultiplexer in order to serialize data from a subset of the data registers onto the memory data bus.

10. The memory module of claim 5, wherein data transfers between one of the data registers and the corresponding rank of memory devices occurs at a clock rate related to the clock rate of the memory data bus by a factor $1/R$.

11. The memory module of claim 5, where the module is a dual-inline memory module comprising a printed circuit board capable of connection to the memory data bus via insertion of the circuit board into a card edge connector connected to the memory data bus.

12. The memory module of claim 11, wherein R equals two, one of the two ranks of memory devices arranged on each side of the circuit board and connected to the corresponding data register via a set of module data signaling lines routed on the circuit board.

13. The memory module of claim 11, where the interface circuit comprises two interface circuits each serving half of the module data port and half of each rank of memory devices.

14. The memory module of claim 5, wherein the module data port comprises a dual-port buffer, each port of the dual-port buffer capable of connection to another memory module in a point-to-point configuration of memory data bus segments.

15. The memory module of claim 14, wherein each port is capable of connection to an *m*-bit-wide memory data bus segment, wherein one port comprises a transfer port and the other port comprises a forwarding port, the module capable of using the transfer port to transfer data signals between the interface circuit and a higher-level controller connected to the memory data bus, the module capable of using the forwarding port to connect to a second memory module in order to transfer data signals between the transfer port on the first memory module and the transfer port on the second memory module.

16. The memory module of claim 14, wherein each module data port is capable of connection to an $m/2$ -bit-wide memory data bus segment, wherein the dual module data ports comprise first and second transfer/forwarding ports, the module capable of retransmitting data signals received at one of the transfer/forwarding ports, but not destined for that memory module, on the other transfer/forwarding port, the module also capable of transferring $m/2$ data signals between each of the transfer/forwarding ports and the interface circuit.

17. The memory module of claim 5, wherein data exchanges over the memory data bus comprise a data strobe signal, the module further comprising a data strobe circuit to generate data strobe signaling when transmitting data over the memory data bus.

18. The memory module of claim 17, wherein the controller begins an internal sequence of interface circuit write operations in response to an externally-supplied data strobe signal.

19. The memory module of claim 5, wherein data exchanges between the interface circuit and the ranks of memory devices comprise a data strobe signal, the module further comprising a data strobe circuit to generate data strobe signaling when transmitting data from the interface circuit to the ranks of memory devices, the interface circuit comprising a register circuit to latch data from the ranks of memory devices based on data strobe signaling received from those devices.

20. A method of host/memory communication comprising:

initiating a data access transaction, involving N data bits, between a memory controller and a memory module;

at the memory module, initiating a corresponding data access transaction between an interface circuit and R ranks of memory devices, each rank capable of m-bit-wide data transfers, R > 1;

transferring the N data bits between the memory controller and the memory module in m-bit-wide data segments; and

transferring the N data bits between the interface circuit and the R ranks of memory devices in $R \times m$-bit-wide segments, where $M = \frac{N}{R \times m}$ is an integer value.

21. The method of claim 20, wherein $N = R \times m$, such that for R data segments transferred between the memory controller and the memory module, one transfer occurs

between the interface circuit and the memory devices.

22. The method of claim 20, further comprising clocking transfers between the memory controller and the memory module at R times the rate that transfers are clocked between the interface circuit and the memory devices.

23. The method of claim 20, further comprising initiating a valid data access transaction when N is an integer multiple of m, but less than $R \times m$.

24. The method of claim 23, wherein when the data access transaction is a write transaction, transferring the N data bits between the interface circuit and N/m of the ranks of memory devices, while signaling the remainder of the ranks to ignore the write transaction.

25. The method of claim 23, wherein when the data access transaction is a read transaction, transferring $R \times m$ data bits, including the N data bits requested for the read transaction, from the R ranks of memory devices to the interface circuit, and transferring the N data bits requested for the read transaction from the memory module to the memory controller.